REMARKS

Claims 1-46 are pending in this application. Claim 9 has been amended to simplify and broaden the preamble language. Claim 15 has been amended to correct a typographical error. New dependent claim 46 has been added to recite the preamble language canceled from independent claim 9. No new matter has been introduced. Applicant acknowledges with appreciation the indication in the October 24, 2005 Office Action that claims 9-12 are allowed. Since only the preamble of claim 9 has been amended, it is submitted that claims 9-12 remain allowed.

Claim 15 stands objected to as "the second conductive layer [of the capacitor] is formed of undoped polysilicon." (October 24, 2005 Office Action at 2). Claim 15 has been amended to recite that the "second conductive layer is formed of doped polysilicon" and to correct, therefore, any perceived unclarity.

Claims 13, 14 and 18-21 stand rejected under 35 U.S.C. §102(b) as being anticipated by Divakaruni et al. (U.S. Patent No. 6,429,068) ("Divakaruni"). This rejection is respectfully traversed.

The claimed invention relates to a method of forming a memory cell. As such, independent claim 13 recites a "method of forming a memory cell" by *inter alia* "forming a transistor including a gate fabricated on a semiconductor substrate and including a source/drain region in said semiconductor substrate disposed adjacent to said gate, said step of forming said transistor including providing a silicide region of said gate." Independent claim 13 also recites "forming a capacitor adjacent said transistor by providing a first conductive layer, a dielectric layer and a second conductive layer." Independent claim 13 further recites that "said steps of providing said first conductive layer, said dielectric layer and said second conductive layer are conducted prior to said step of providing said silicide region of said gate."

Divakaruni relates to a "process for fabricating embedded vertical DRAM cells" that includes "fabricating vertical MOSFET DRAM cells with silicided polysilicon layers in the array regions, the landing pad and/or interconnect structures, the support source and drain regions and/or the gate stack." (Abstract). According to Divakaruni, "[T]he process eliminates the need for a M0 metallization layer." (Abstract).

Divakaruni fails to anticipate the subject matter of claims 13, 14 and 18-21. Divakaruni does not disclose, teach or suggest "forming a transistor including a gate fabricated on a semiconductor substrate and . . . *providing a silicide region of said gate*," as in the claimed invention (emphasis added). Divakaruni first teaches that a buried transistor gate is fabricated below a surface of semiconductor substrate 202 so that "array gate polysilicon layer 220 is separated from an underlying deep trench polysilicon region 230 by a trench top oxide layer 226." (Col. 7, lines 40-46; Fig. 4). Divakaruni then teaches that a silicide region is formed as part of its memory array. However, "metal conductor layer 252" of Divakaruni (which could be a tungsten silicide/tungsten layer) is "used to form the wordline stack in the array region" (col. 8, lines 47-52) and, thus, is not a silicide region of a gate, as in the claimed invention.

Applicant further notes that Divakaruni fails to disclose, teach or suggest the step of "forming a capacitor adjacent said transistor by providing a first conductive layer, a dielectric layer and a second conductive layer," much less that "said steps of providing said first conductive layer, said dielectric layer and said second conductive layer are conducted prior to said step of providing said silicide region of said gate," as independent claim 13 also recites. Divakaruni is silent about the formation of a capacitor structure, or about the specific steps of forming a capacitor prior to the formation of a silicide layer that is an integral part of a gate structure, as in the claimed invention.

The assertion in the October 24, 2005 Office Action that layers 230, 226 and 220 of Divakaruni correspond to the first conductive layer, the dielectric layer and the second conductive layer of the claimed invention is unsupported. As noted above, layers 230, 226 and 220 of Divakaruni correspond to the embedded gate structure, and not to a capacitor. Divakaruni clearly teaches that the transistor gate is fabricated below a surface of semiconductor substrate 202 so that "array gate polysilicon layer 220 is separated from an underlying deep trench polysilicon region 230 by a trench top oxide layer 226." (Col. 7, lines 40-46; Fig. 4).

For at least the reasons above, the subject matter of claims 13, 14 and 18-21 is not anticipated by Divakaruni, and withdrawal of the rejection of these claims is respectfully requested.

Allowance of the application is solicited.

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Respectfully submitted,

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